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APPLICATION NO.	FI	LING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,743	10/692,743 10/27/2003		Takayuki Matsui		60188-691 8873	
	7590	10/03/2006			EXAM	INER
Jack Q. Lever, Jr. McDERMOTT, WILL & EMERY					WEINMAN	, SEAN M
	600 Thirteenth Street, N.W.				ART UNIT	PAPER NUMBER
Washington, DC 20005-3096					2115	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)					
	10/692,743	MATSUI ET AL.					
Office Action Summary	Examiner	Art Unit					
	Sean Weinman	2115					
The MAILING DATE of this communication app	ears on the cover sheet with the c	orrespondence address					
Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
1)⊠ Responsive to communication(s) filed on <u>amen</u>	ndment filed on July 18, 2006						
,	Responsive to communication(s) filed on <u>amendment filed on July 18, 2006</u> . This action is FINAL . 2b) This action is non-final.						
,		secution as to the merits is					
	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
diosed in absorbance with the practice and of E	A pullo Quaylo, 1000 0.5. 11, 10	, 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0					
Disposition of Claims							
4) Claim(s) 1-20 is/are pending in the application.	4) Claim(s) 1-20 is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.							
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1-20</u> is/are rejected.	☑ Claim(s) <u>1-20</u> is/are rejected.						
7) Claim(s) is/are objected to.	Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or	r election requirement.						
Application Papers							
9) The specification is objected to by the Examiner. 10) The drawing(s) filed on 18 July 2006 is/are: a) accepted or b) objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C. § 119							
	majority under 25 H C C \$ 110/o) (d) or (f)					
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
a)⊠ All b)☐ Some * c)☐ None of: 1.⊠ Certified copies of the priority documents have been received.							
 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 							
Copies of the certified copies of the priority documents have been received in Application No Copies of the certified copies of the priority documents have been received in this National Stage							
application from the International Bureau (PCT Rule 17.2(a)).							
* See the attached detailed Office action for a list of the certified copies not received.							
Gee the attached detailed effice detail for a list of the defining depice not received.							
Attachment(s)							
Attachment(s) 1) Notice of References Cited (PTO-892)	4) Interview Summary	(PTO-413)					
2) Notice of Profeseinces Orice (175 032) Notice of Draftsperson's Patent Drawing Review (PTO-948)	ate						
3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 5) Notice of Informal Patent Application 6) Other:							
Paper No(s)/Mail Date 6) LJ Other:							

Application/Control Number: 10/692,743

Art Unit: 2115

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DETAILED ACTION

This action is responsive to the amendment filed on July 18, 2006. Claims 1-20 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission of Prior Art (AAPA) in view of Chang et al. (US Patent Application Publication 2003/0101311) in further view of Veendrick (US Patent No. 6,081,149

As per claims 1, 9, 11, and 19, the AAPA teaches the claimed invention comprising:

A data transmission system for carrying out a serial data transmission based on IEEE 1394 standard, the system comprising: an interface control semiconductor integrated circuit for controlling the serial data transmission (Figure 9 and page 2 lines 7-11), the interface control semiconductor integrated circuit including a plurality of protocol circuits (Figure 9 and page 2 lines 7-20).

The AAPA, however, does not teach that the interface control semiconductor integrated circuit includes a plurality of switches to control the clock of each of the protocol circuits.

Additionally, the AAPA does not teach that there is a determination means for controlling the clock of the protocol circuit based on the 1394 control information from the interface control.

Art Unit: 2115

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Specifically, the AAPA teaches an interface control semiconductor integrated circuit having a plurality of protocol circuits supplied by a clock that control the data transmission in a data transmission system. The AAPA does not teach switches for controlling the clock of the protocol switches and also does not teach a determination means for controlling the switches based on 1394 control information.

Chang et al. teaches a 1394 bus system which obtains information from the 1394 bus interface and then makes a determination whether to adjust the clock of the integrated circuits within the bus interface to reduce the power consumed by the system. Chang et al. teaches the invention comprising determination means for obtaining 1394-control-information from the interface control semiconductor integrated circuit and making a determination whether to supply or shut off a clock with respect to each of the protocol circuits based on the 1394-control-information (*Paragraph [0076]*). In summary, Chang et al. teaches a 1394 bus system that obtains 1394 control information from the interface and then a processor determines whether or not to control the clock of the various integrated circuit within the interface to reduce the power consumed by the system. Chang et al. not teach switches for controlling the clock of the protocol switches.

Veendrick teaches a plurality of switches that control a clock signal with their respective circuits for reducing the power consumed in a system. Veendrick teaches the claimed invention comprising a plurality of switches associated with the respective protocol circuits, each of the switches performing a switching between supply and shut-off of a clock (Figure 1 and Col. 2 lines 20-32 and lines 41-46). In summary, Veendrick teaches a plurality of circuits having corresponding switches, which control the function of a common clock, to reduce the power

Application/Control Number: 10/692,743

Art Unit: 2115

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consumed of a circuit. Additionally, Veendrick teaches a controller which determines the specific function of the clock for the specific circuits.

Page 4

It would have been obvious to one of ordinary skill in the art to combine the teaching of the AAPA and Chang et al. because they both teach 1394 bus system with 1394 bus interfaces to control the data transmitted in the system. Chang et al. covers the deficiency of the AAPA by teaching that 1394 bus system obtains information from the 1394 bus interface and then makes a determination whether to adjust the clock of the integrated circuits within the bus interface.

Additionally, it would have been obvious to one of ordinary skill in the art to combine Veendrick with Chang et al. because they both teach method of reducing the power consumption of system by controlling the clock of individual circuits within that system. Veendrick covers the deficiency of Chang et al. by teaching a plurality if switches used to control the clock signal of individual circuit within the system. One of ordinary skill would have been motivated to combine the teachings of AAPA, Chang et al., and Veendrick because they all teach systems which would hekp further reduce the power consumption of a 1394 bus system.

As per claims 2 and 10, Veendrick teaches the claimed invention comprising:

a clock control register for holding control information on the switches (Figure 1 and Col. 2 lines 20-32 and lines 41-46 It would be obvious to one of ordinary skill in the art that a register to hold control information must exist for the clock controller know the status and control information of the switches); and

a clock selector for controlling operation of the switches based on the control information

(Figure 1 and Col. 2 lines 20-32 and lines 41-46), and

Application/Control Number: 10/692,743 Page 5

Art Unit: 2115

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the determination means updates the control information held in the clock control register, based on the determination (It would be obvious to one of ordinary skill in the art that the determination means updates the register so that the clock controller would know the current statuses of the switches).

As per claims 3 and 13, Chang et al. teaches the claimed invention comprising:

determination means makes the determination based on the number of nodes (Paragraph [0076] Chang et al. does not explicitly teach the determination based on the number of nodes but it would be obvious to one of ordinary skill in the art that for the interface to anticipate an increase in bus traffic that the interface would makes it determination of whether to enter a power consumption mode based on the number of nodes and work within the system).

As per claims 4 and 14, Chang et al. teaches the claimed invention comprising:

determination means analyzes the packet and makes the determination based on a result

of the analysis (Paragraph [0006] and [0076]).

As per claims 4-8 and 14-18, Chang et al. teaches the claimed invention comprising:

determination means makes a determination to supply a clock to one of the protocol

circuits engaged in the data transmission, before/after a first/last packet has been sent or received

in a transaction (Paragraph [0006] and [0076] Chang et al. does not explicitly teach controlling

the clock of the protocol circuits before/after the first/last packet has been sent but it would have

been obvious to one of ordinary skill that since the determination of the power consumption

mode is based on the traffic that the system would enter and exit the power consumption mode

based on the timing of the first and last packets).

Art Unit: 2115

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As per claims 12-18 and 20, it is directed to the method of controlling the protocol circuit in the interface control semiconductor integrated circuit in the data transmission system as set forth in claims 1-8 and 19. Since the AAPA, Chang et al., and Veendick teach the claimed data transmission system with the protocol circuit in the interface control semiconductor integrated circuit, the AAPA, Chang et al., and Veendick teach the method of controlling the interface control semiconductor integrated circuit in the data transmission system.

Response to Arguments

Applicant's arguments filed on July 18, 2006 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., determining the type of data to be transmitted and then utilizing this information to determine which protocol circuit should be provided with a clock signal) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In the remarks, applicant argues that Chang does not disclose or suggest, determining the type of data to be transmitted and then utilizing this information to determine which protocol circuit should be provided with a clock signal. The examiner respectfully disagrees with applicant's position. As stated above, the claims do not recite determining the type of data to be transmitted and then utilizing this information to determine which protocol circuit should be provided with a clock signal.

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Page 7

Additionally, applicant argues that the fact the prior could be modified would not have made the modification obvious unless the prior art suggests the desirability of the modification. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation to combine is stated in the rejection hereinabove.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Application/Control Number: 10/692,743 Page 8

Art Unit: 2115

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Weinman whose phone number is (571) 272-2744. The examiner can normally be reached on Monday-Friday from 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sean Weinman Examiner Art Unit 2115

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